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(formerly S01022.80707.US)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ferruccio Frisina
Serial No.: 09/925,080
Filed: August 8, 2001
For: METHOD OF MANUFACTURING AN INTEGRATED EDGE
STRUCTURE FOR HIGH VOLTAGE SEMICONDUCTOR DEVICES,
AND RELATED INTEGRATED EDGE STRUCTURE
Confirmation No.: 3073
Examiner: Luu, Chuong A.
Art Unit: 2825

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 15, 2003.



Jeanne Spinelli

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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AMENDMENT

Sir:

In response to the Office Action mailed July 14, 2003, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the Listing of Claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.